REMARKS

Claims 1, 3-8, and 10-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over combinations of U.S. Patent Application Publication No. 2002/0063671 to *Knapp* ("*Knapp*"), U.S. Patent No. 6,236,388 to *Iida et al.* ("*Iida*"), and Japanese Patent No. JP 2000-310767 to *Park et al.* ("*Park*"). Applicants respectfully traverse, noting that no reference discloses every element of these claims. More specifically, no reference discloses simultaneous sequential scanning of gate lines in first and third areas. Additionally, no reference discloses providing the same data voltages to pairs of data lines while second areas are scanned.

First, no reference discloses sequential scanning of gate lines from first and third areas. As noted by Examiner, *Knapp* does not disclose simultaneous sequential scanning of gate lines from first and third areas (Office Action, p. 4). *Iida* does not cure this deficiency in *Knapp*. Examiner asserts that *Iida* discloses scanning of "first" and "third" areas simultaneously (Id.). Even if true, *Iida* does not disclose that either area is scanned sequentially. At most, *Iida* only states as follows:

> FIG. 5 shows a writing timing of a black signal in the vertical scanning circuit shown in FIG. 4. A part of the transferring stage included in the vertical scanning circuit of the display panel is simultaneously operated during the vertical blanking period of the image signals in order to collectively write the black signal VBLK to the upper-side and lower-side rows of the blank area. That is, the timing generator supplies a single pulse signal BCPX during the vertical blanking period. The vertical scanning circuit on the display panel side simultaneously outputs BPCX in place of the selection pulse Φ_V to the gate lines X corresponding to the upper-side and lower-side rows, causing the black signal VBLK to be collectively written to all the upper-side and lower-side rows. After this vertical blanking period has elapsed, the display panel enters a normal operation, and the image signals VSIG and the black signal VBLK are written to the pixels for one row every horizontal period in a column-divided manner. In this way, in this example, the upper-side and lower-side rows of the blank area are selected collectively in a specific time (output time of BCPX) within the vertical blanking period, and at the same time the black signal VBLK is written to the pixels in the upper-side and the lower-side rows.
>
> (*Iida*, Cols. 9:56-10:10 (emphases added))

As can be seen, *Iida* never discloses that its upper-side and lower-side rows are scanned sequentially. Indeed, from the underlined portions, *Iida* seems to imply that the gate lines of its

upper-side and lower-side rows are all scanned simultaneously, not sequentially. Accordingly, *Iida* does not disclose simultaneous sequential scanning of gate lines from first and third areas.

Park also does not disclose sequential scanning of gate lines from first and third areas. Applicants' claim 1 is thus patentable over each of these references for at least the reason that it recites "wherein the first gate lines are sequentially scanned while the third gate lines are sequentially scanned." Similarly, claim 12 is patentable over each of these references for at least the reason that it recites "the first gate lines being sequentially scanned while the third gate lines are sequentially scanned." The remaining claims each depend from one of claims 1 and 12, and are thus also patentable for at least these same reasons.

Second, no reference discloses providing the same data voltages to pairs of data lines while second areas are scanned. Examiner asserts that ¶[0029] of *Knapp* contains such a disclosure. Respectfully, this is incorrect. This portion of *Knapp* only states as follows:

> **[0029]** Because the sub-matrices defined by splitting the column conductors do not now each comprise a whole number of complete pixel rows, but instead include respective pixels from the same group of rows around the middle of the array, both the column driver circuits 35A and 35B will need to be operating when this group is being addressed. The periods for which the circuits are powered up is, therefore, extended slightly so that both are active while the rows K to K+X are being addressed. The active periods of the two circuits 35A and 35B will thus overlap to a small extent, as shown in the control timing diagram in FIG. 3 where Tb indicates the overlap period. However, as the number of pixels rows constituting the group is comparatively low, then the fraction of the total field period for which both circuits are operating simultaneously will be very small. The driver circuits thus still operate substantially alternately, in consecutive time periods and the increase in power consumption in this embodiment compared to the previous embodiment will be minimal.
> (*Knapp*, ¶[0029] (emphases added))

As can be seen, *Knapp* at most only discloses that the two driver circuits are powered up at the same time. This falls short of disclosing that these two circuits actually apply voltages at the same time. Additionally, this portion of *Knapp* does not disclose that the driver circuits 35A, 35B ever apply the same data voltages.

Accordingly, *Knapp* does not disclose actually providing voltages to pairs of data lines while second areas are scanned, nor does *Knapp* disclose applying the same data voltages to pairs of data lines. Neither *Iida* nor *Park* cures this deficiency in *Knapp*, as neither appears to

disclose the scanning of the second of three areas while also providing the same data voltages to pairs of data lines.

Claim 1 is thus patentable over each of these references for at least the additional reason that it recites "wherein same data voltages are provided on the data lines of each pair while the respective second gate lines are scanned." Similarly, claim 12 is patentable over each of these references for at least the additional reason that it recites "after the applying data voltages for each first pixel and each third pixel, sequentially applying scanning signals to the second gate lines; and applying same data voltages for each second pixel to both the respective first and second data lines." The remaining claims each depend from one of claims 1 and 12, and are thus also patentable for at least these same additional reasons.

CONCLUSION

For the reasons stated above, Claims 1, 3-8, and 10-15 are now in condition for allowance. The Director is hereby authorized to charge any deficiency in fees, or credit any overpayment, to Deposit Account No. 50-5029. Please telephone the undersigned attorney at (408) 331-1671 if there are any questions.

Respectfully submitted,

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